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(54) **INTEGRATED START-UP BIAS BOOST FOR DYNAMIC ERROR VECTOR MAGNITUDE ENHANCEMENT**

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See application file for complete search history.

(71) Applicant: **MICROSEMI CORPORATION**, Aliso Viejo, CA (US)

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*Primary Examiner* — Khanh V Nguyen

(74) *Attorney, Agent, or Firm* — Marger Johnson

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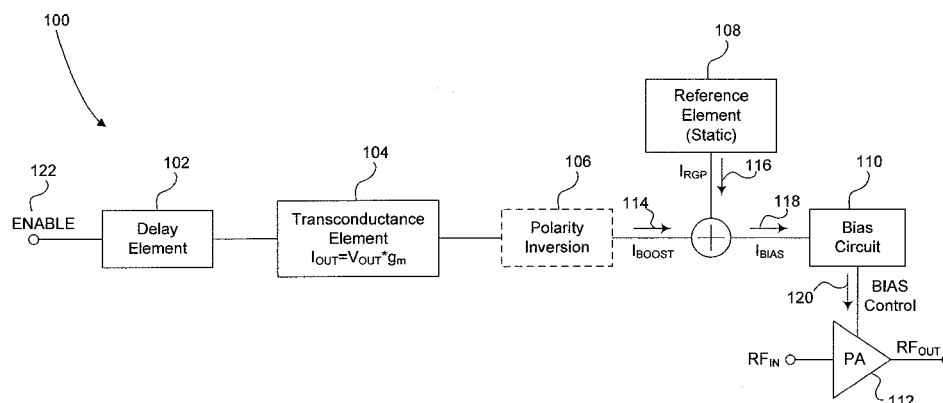
(57) **ABSTRACT**

Devices and methods for correcting for start-up transients in integrated power amplifiers are disclosed. A delay element is arranged to produce a delay waveform signal that is responsive to an input voltage signal. A transconductance element has an input that receives the delay waveform signal and is arranged to provide an output boost current that is based on the delay waveform signal and a gain of the transconductance element. A reference element provides an output bias current that is responsive to a static reference current and the boost current. A bias element has an input that receives the bias current and is arranged to provide a bias control output. A power amplifier is responsive to the bias control output and is arranged to provide an amplified power output.

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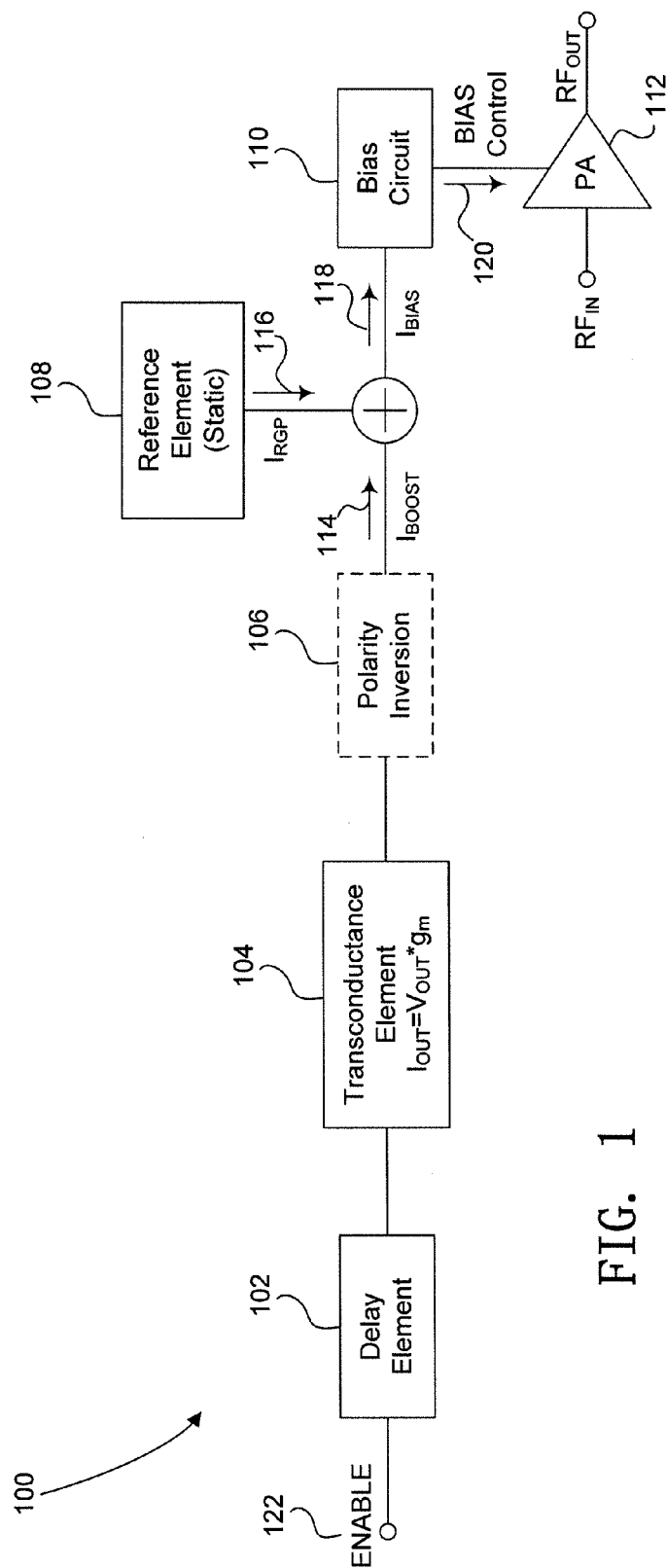


FIG. 1

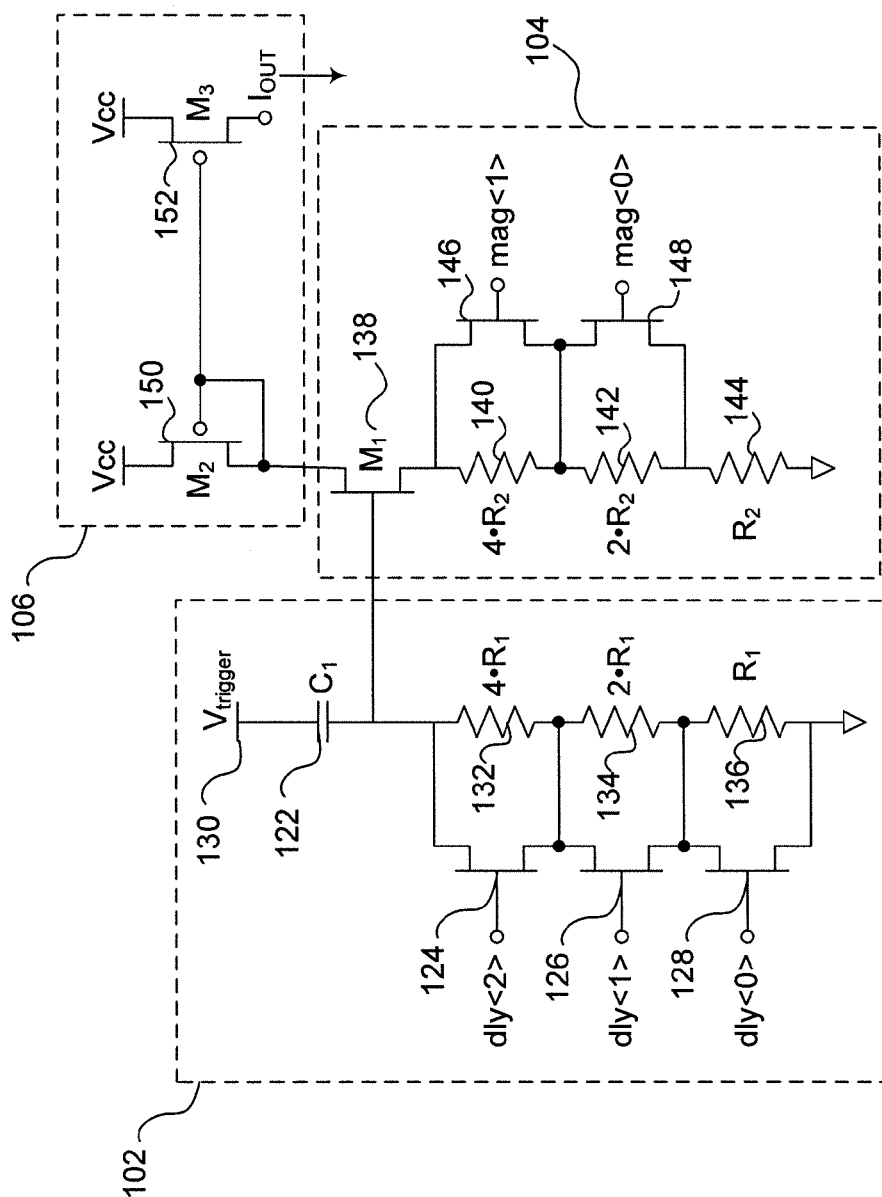


FIG. 2A

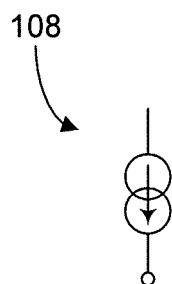


FIG. 2B

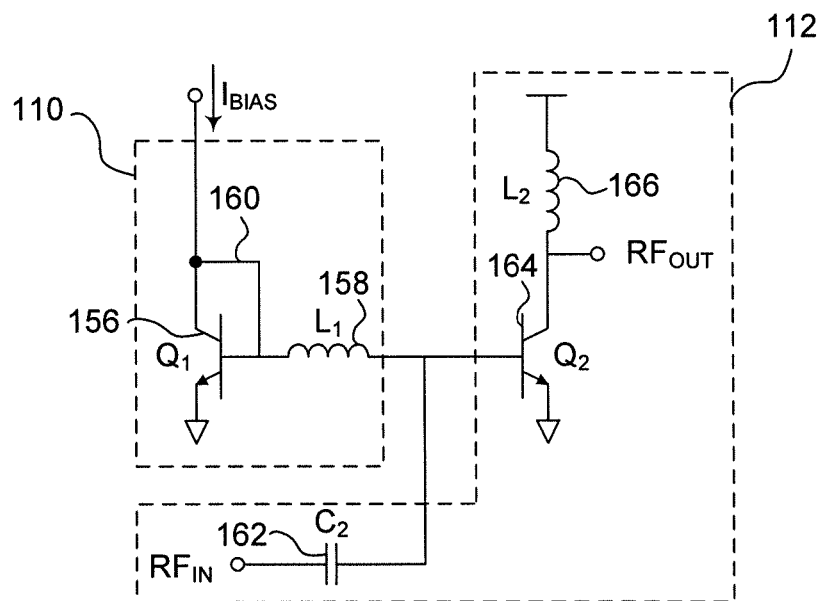


FIG. 2C

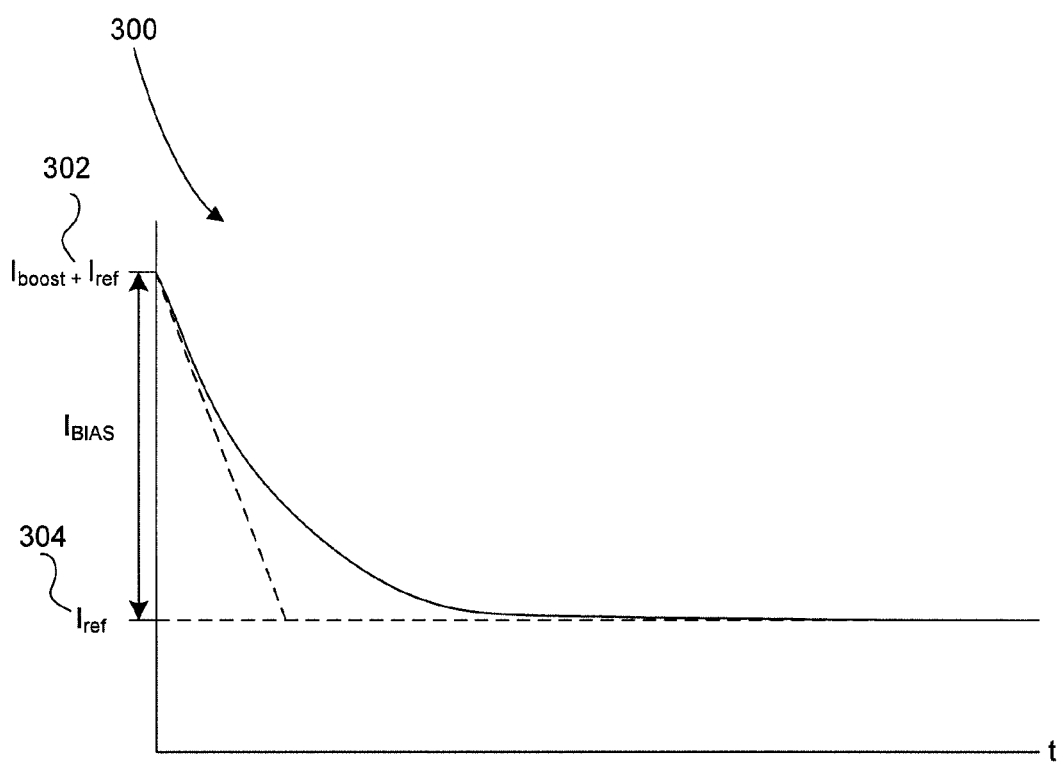


FIG. 3

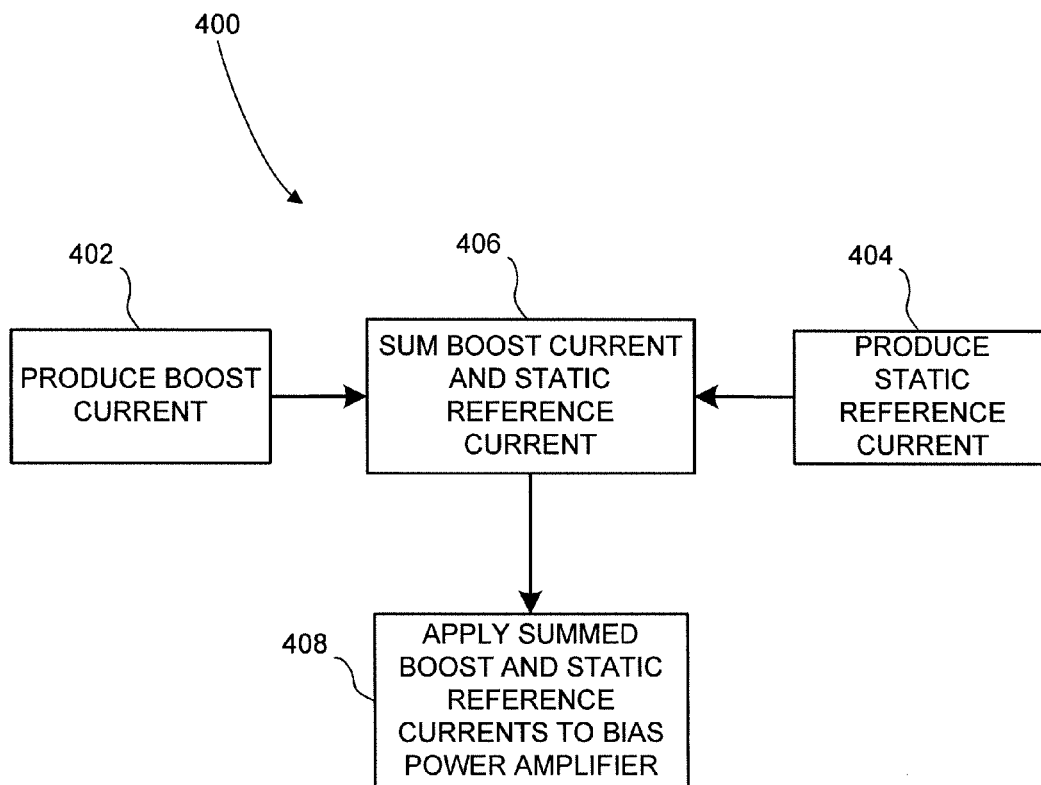


FIG. 4

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# INTEGRATED START-UP BIAS BOOST FOR DYNAMIC ERROR VECTOR MAGNITUDE ENHANCEMENT

## CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional application Ser. No. 61/648,504, filed May 17, 2012, herein incorporated by reference.

## FIELD OF THE INVENTION

This disclosure relates to enhancing power amplifier performance and more particularly to enhancing power-on performance of a power amplifier in an integrated circuit.

## BACKGROUND OF THE INVENTION

Power amplifiers may be integrated onto the same die as receiving or other types of amplifiers in many communications standards, such as wireless LAN. A switch permits transmission of signals through the antenna to/from either the power amplifier circuit or the receiving or other amplifier, depending on the needs of the communications circuit. When the power amplifier is transmitting signals, power is supplied to the power amplifier. When the power amplifier is not actively transmitting signals, power is not supplied to the power amplifier. Upon powering on, the power amplifier experiences a period of time during which the signal that is transmitted is changing and the transmission characteristics of the power amplifier are also changing, which is difficult to train or characterize by other circuit components or other circuits coupled to the power amplifier circuit. In some circumstances such as Wireless LAN, the receiving circuit that receives the signal transmitted from the power amplifier is arranged to determine the characteristics of the incoming signal from the power amplifier within a finite period of time after which the receiving circuit assumes that the signal changes remain consistent upon further receipt of the signal over time.

The time period during which the receiving circuit determines the characteristics of the incoming signal from the power amplifier may be relatively short, approximately 4  $\mu$ s in some wireless LAN examples, compared to the time period during which the power amplifier is powering on and during which the transmission characteristics of the power amplifier signal are changing and the manner in which they are changing is also changing. This assumption of no further changes to the manner in which the signal is changing leads to the receiving circuit assuming that the power amplifier signal is not continuing to change in the same manner when in fact the characteristics of the power amplifier signal are continuing to change, which can lead to inaccuracies in how the signal is being processed by the receiving circuit.

To accommodate for changing transmission characteristics during the powering-on time period of the power amplifier, a reference circuit has been coupled to the power amplifier to generate a complementary reference current to the current flowing through the power amplifier. The complementary reference current produced by the reference circuit has an input of a voltage from a control source that is then converted to the reference current by the reference circuit. A reference circuit resistor sets both the steady state current value and the time constant or delay. A reference circuit capacitor value becomes fixed as a result of the fixed value for the reference circuit resistor. The steady state current value requires that the

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capacitor value be relatively large and that value can be upwards of 100 nF in some examples. It is not practical for such a large capacitor to be physically present on die and therefore it must be located off-die.

Therefore, improvements that correct for the powering-on or start-up transients that power amplifiers inherently experience that are both size and cost efficient are desirable in the art.

## SUMMARY OF THE INVENTION

An object of this invention is to provide methods and device structures suitable for correcting for start-up transients in power amplifiers.

An example circuit that corrects for start-up transients in power amplifiers includes a delay element, a transconductance element, a reference element, a bias element, and a power amplifier. The delay element is arranged to produce a delay waveform signal that is responsive to an input voltage signal. The transconductance element has an input that receives the delay waveform signal from the delay element and is arranged to provide an output boost current that is based on the delay waveform signal and a gain of the transconductance element. The reference element provides an output bias current that is responsive to a static reference current and the boost current. The bias element has an input that receives the bias current and is arranged to provide a bias control output. The power amplifier is responsive to the bias control output and is arranged to provide an amplified power output. The power amplifier provides a first amount of power gain during a first time period after the power amplifier is powered on and a second amount of power gain during a second time period following the first time period after the power amplifier is powered on. The first amount of power gain is responsive to the sum of the boost current and the static reference current. The second amount of power gain is determined by decay of the output bias current to a value of the static reference current.

Methods of correcting for a start-up transient in a power amplifier include producing a boost current having a decay characteristic, producing a static reference current, summing the boost current and the static reference current, and applying the summed boost current and the static reference current to bias the power amplifier.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of embodiments of the invention which proceeds with reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is block diagram that corresponds to elements of an integrated start-up bias boost circuit for a power amplifier, according to embodiments of the disclosure.

FIG. 2A is a schematic of an example a delay waveform, transconductance element, and optional polarity inverter of an integrated start-up bias boost circuit for a power amplifier in accordance with aspects of the disclosure.

FIG. 2B is a schematic of an example bias reference element of an integrated start-up bias boost circuit for a power amplifier, according to aspects of the disclosure.

FIG. 2C is a schematic of an example bias circuit and a power amplifier of an integrated start-up bias boost circuit for a power amplifier, in accordance with aspects of the disclosure.



FIG. 3 is a graphical representation of bias current over time, according to aspects of the disclosure.

FIG. 4 shows steps in a method of correcting for a start-up transient in a power amplifier, in accordance with aspects of the disclosure.

#### DETAILED DESCRIPTION

In the drawings, which are not necessarily to scale, like or corresponding elements of the disclosed systems and methods are denoted by the same reference numerals.

To correct for start-up transients inherent in power amplifiers, such as the LX5585 and LX5590 power amplifiers manufactured by Microsemi Corporation®, the disclosed circuits and methods provide for separating the circuit elements used to set the delay from those circuit elements used to set the output magnitude of the bias current and the characteristics of the output signal of the power amplifier. By separating the delay and the output magnitude of the bias current, the output signal of the power amplifier compensates for the start-up transients inherent in power amplifiers, in many environments, specifically in a monolithic solution for example. This arrangement provides adjustable control mechanisms and the ability to control the circuit's behavior in any standard CMOS/BiCMOS process.

Referring now to FIG. 1, a circuit that corrects for start-up transients in power amplifiers **100** is illustrated in a block diagram. The circuit includes a delay element **102**, a transconductance element **104**, a reference element **108**, a bias element **110**, and a power amplifier **112**. Optionally, the correcting circuit **100** can also include a polarity inversion circuit **106**. The delay element **102** is arranged to produce a delay waveform signal that is responsive to an input signal. In other examples, a switch of any kind can generate the input voltage signal that is received at the input of the transconductance element **104**. The transconductance element **104** has an input that receives the delay waveform signal from the delay element **102** and is arranged to provide an output boost current ( $I_{BOOST}$ ) **114** that is based on the delay waveform signal and a gain of the transconductance element **104**. The reference element **108** may be a bias reference element that provides a static reference current ( $I_{RGP}$ ) **116**. The currents  $I_{BOOST}$  and  $I_{RGP}$  are summed to produce an output bias current ( $I_{BIAS}$ ) **118** that is received as the input to the bias circuit **110**. The bias circuit **110** produces a bias control output **120** based on  $I_{BIAS}$ . The power amplifier **112** is responsive to the bias control output and is arranged to provide an amplified power output.

The power amplifier **112** shown in FIG. 1 provides a first amount of power gain during a first time period after the power amplifier is powered on and a second amount of power gain during a second time period after the power amplifier is powered on. The second time period is after the first time period in this example. The first amount of power gain is responsive to the sum of  $I_{BOOST}$  and  $I_{RGP}$ . The second amount of power gain is determined by the decay of the output bias current  $I_{BIAS}$  portion of the output control bias toward a value of the static reference current,  $I_{RGP}$ , which occurs over time. For example, the first time period and the second time period extend over about 100  $\mu$ s after the power amplifier is powered on. The first time period may begin when an enabling control signal **122** is supplied to the power amplifier, in some examples, which may be concurrent with or slightly before or after the power amplifier is powered on. At the end of the first time period, the output bias current  $I_{BIAS}$  value of the bias control output has peaked in value and has decayed toward the value of the static reference current  $I_{RGP}$ .

The transconductance element **104** of the block diagram of the start-up bias boost circuit **100** illustrated in FIG. 1 converts the delay waveform signal that it receives at its input into an output current with an output gain. In some examples, the delay waveform signal includes a delay waveform voltage that is converted to an output current by the transconductance element **104**. Optionally, the output current of the transconductance element **104** is received as input to a polarity inversion circuit **106**. The polarity inversion circuit **106** can turn a current sink into a current source. For example, when the transconductance element **104** outputs a current that needs amplifying, then the current is transmitted through the polarity inversion circuit **106**, or current mirror circuit, to amplify the current to its maximum value. When the output current of the transconductance element **104** is correct, such as being equal to its maximum value, then the polarity inversion circuit **106** can be bypassed. Regardless, the output current of the transconductance element **104**, whether or not it passes through the polarity inversion circuit **106**, produces the output boost current,  $I_{BOOST}$  **114**. In the examples in which the output current of the transconductance element **104** is transmitted through the polarity inversion circuit **106**, the polarity inversion circuit receives the boost current from the output of the transconductance element **104** and is arranged to provide an output current that is a mirrored boost current. The mirrored boost current or simply the boost current is depicted as  $I_{BOOST}$  in FIG. 1.

The output bias current,  $I_{BIAS}$ , is responsive to  $I_{BOOST}$  or the mirrored boost current, depending on whether the current is transmitted through the polarity inversion circuit **106**. In the examples in which the current is transmitted through the polarity inversion circuit **106**, the output bias current,  $I_{BIAS}$ , is the sum of the static reference current,  $I_{RGP}$ , and the mirrored boost current. In the examples in which the current bypasses the polarity inversion circuit **106**, the output bias current,  $I_{BIAS}$ , is the sum of the static reference current  $I_{RGP}$  and the boost current output from the transconductance element **104**.

FIGS. 2A-2C show example schematics of some elements of the start-up bias boost circuit **100** discussed in FIG. 1. These are examples and other embodiments of these circuits may be implemented in accordance with this disclosure. FIG. 2A is an example schematic of a delay element **102**, a transconductance element **104**, and a polarity inversion circuit **106**. The delay element **102** can be a resistor-capacitor (RC) charge circuit, in some examples, in which a capacitor **122** begins to charge when the trigger voltage input **130** transitions from low (0V) to high. A combination of the delay switches **124**, **126**, **128** are closed to select one of delays d0, d1, or d2. The voltage input **130** to the delay element **102** ranges from 0V when voltage is not being supplied to the delay element **102** to approximately 3.3V when voltage is supplied to the delay element **102** and the capacitor **122** begins to charge the RC charge circuit, for example. In alternative examples, the delay element can include one or more simple switches or other circuit elements that provide power to the start-up bias boost circuit.

In the example shown in FIG. 2A, the delay element **102** includes the capacitor **122** and a series of digitally controllable resistors **132**, **134**, **136** electrically coupled together in series. However, in alternative examples, the capacitor and may be electrically coupled to a single resistor or any other suitable number of resistors. In addition, switching elements may be used in combination with multiple capacitors to provide adjustable delays. Again referring to FIG. 2A, the series of resistors **132**, **134**, **136** are digitally selectable by their respective switches **124**, **126**, **128**, such as field effect transistors (FETs) for example, or any other suitable switch. In

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this example, when FETs **124**, **126** are closed (conducting) and FET **128** is open (non-conducting), the resistance of the delay element **102** becomes the value of  $R_1$ . When FETs **124**, **128** are closed and FET **126** is open, the resistance becomes the value of  $2 \cdot R_1$ , in this example. When FETs **126**, **128** are closed and FET **124** is open, the resistance of the delay element **102** becomes the value of  $4 \cdot R_1$ , in this example. By varying the FETs **124**, **126**, **128** that are open and closed, the resistance value of the delay element **102** can be controlled. By controlling the resistance value of the delay element **102**, the delay waveform signal's response to the input voltage signal received by the delay element **102** can also be controlled.

The output voltage signal of the delay element **102** is received at the input of the transconductance element **104**, which produces an output boost current. The transconductance element **104** includes an amplifying device **138** or transistor and a series of resistors **140**, **142**, **144** electrically coupled together in series. In the example transconductance element **104** shown in FIG. 2A, the amplifying device **138** is a FET, for example, or can be any other suitable type of amplifying device. The resistors **140**, **142**, **144** can be one large resistor in other examples. However, in FIG. 2A, the resistors **140**, **142**, **144** are a series of three digitally selectable resistors electrically coupled together in series. These resistors **140**, **142**, **144** are digitally controlled by two switches **146**, **148** that vary the resistance and thus the output boost current that is output from the transconductance element **104**. The transconductance element **104** has a minimum resistance of  $R_2$  that may increase depending on whether one or both of the switches **146**, **148** are open or closed.

The output boost current of the transconductance element **104** is received as input to the polarity inversion circuit **106** shown in FIG. 2A. The polarity inversion circuit **106** includes two metal oxide semiconductor field effect transistors **150**, **152** (MOSFETs), in this example, electrically coupled in series to each other. The polarity inversion circuit **106** generates a mirrored output boost current that is greater than, but directly proportional to the boost current output by the transconductance element **104**.

FIG. 2B is an example reference element **108**. The reference element **108** can be a static reference element that is arranged to provide a static reference current that sets an operating parameter of the power amplifier, namely the current that flows through the power amplifier's bipolar transistor.

Turning now to FIG. 2C, example schematics of the bias circuit **110** and the power amplifier **112** are shown. The bias circuit **110** receives the summed bias current of the output boost current, the output current from FIG. 2A, and the static reference current, the output current from FIG. 2B. The bias circuit **110** shown in FIG. 2C includes a bipolar transistor **156** and an inductor **158** electrically coupled in series with each other. A bypass pathway **160** couples the gate to the collector of the bipolar transistor **156**, thus effectively turning the bipolar transistor **156** into a diode. The bias circuit **110** provides an elevated bias voltage to the power amplifier **112** when the power amplifier **112** is powered on, which helps to correct for the changes in performance characteristics of the power amplifier **112** during the powering on time period.

FIG. 2C also shows an example schematic of a power amplifier **112** having a capacitor **162**, a bipolar transistor **164**, and an inductor **166**. An input signal to the power amplifier **112** is a radio frequency (RF) input and the output of the power amplifier **112** is an RF output signal that is amplified by a gain defined by the power amplifier **112**. When the power amplifier **112** is powered off, the current through the bipolar

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transistor **164** of the power amplifier **112** is essentially zero. When the power amplifier **112** is powered on, the current through the bipolar transistor **164** rapidly changes and then gradually approaches its steady state value. During the time period when the current through the bipolar transistor **164** is changing, the RF characteristics of the power amplifier **112** are also changing. The steady state value of the current through the bipolar transistor **164** of the power amplifier **112** is proportional to the value of the static reference current **116**. The bias control current is a current boost that, when summed with the static reference current and input into the power amplifier **112**, helps to correct for the changes to the RF characteristics of the power amplifier **112** when it is powered on during its "transient" period, which otherwise has a negative impact on the overall system performance.

The bias circuit **110** generates the bias voltage for the bipolar transistor **164** of the power amplifier **112**. The operating point of the bipolar transistor **164** of the power amplifier **112** is set by the static reference current that flows through the reference device **156** of the bias circuit **110**. As discussed above, the input current to the bias circuit **110** is generated by summing the static reference current and the output current boost. When the power amplifier **112** is powered off, the control voltage **130** to the start-up bias boost circuit **100** is brought to ground, which resets the circuit **100** in the examples shown in FIGS. 1-2C. In alternative embodiments, the circuit **100** can have a constant supply voltage (although the value of the supply voltage may vary) and the circuit can be reset through other ways, such as FET switches.

In the examples shown in FIGS. 2A-2C, the start-up bias boost circuit **100** has two design equations:

$$t_{delay} = (R_1 \cdot C_1) \text{ seconds}$$

$$I_{BOOST,max} = (V_{CC} - V_{M1}) / R_2 \text{ amps}$$

These design equations have three degrees of freedom— $C_1$ ,  $R_1$ , and  $R_2$ .  $C_1$  is the capacitor **122** included in the delay element **102** of the start-up bias boost circuit **100** and is generally fixed by layout constraints and can be chosen to be as large as conventionally possible. To achieve the desired delay, which is in the range of 100's of  $\mu$ s,  $R_1$  corresponding to the resistance value **132**, **134**, **136** of the delay element **102** also tends to be relatively large, such as 2 M $\Omega$ . To achieve the desired magnitude of the output boost current, the value of  $R_2$  corresponding to the resistance value **140**, **142**, **144** of the transconductance element **104** can be chosen independently of  $R_1$  and  $C_1$ . All three degrees of freedom,  $C_1$ ,  $R_1$ , and  $R_2$ , are controllable to change the value of the desired delay and the output boost current.

As discussed above, before the power amplifier **112** is powered on, the control voltage **130** to the delay element **102** is zero, which means that all node voltages are also zero and the static reference current is zero. The diode **156** in the bias circuit **110** and the bipolar transistor **164** in the power amplifier **112** are off and the voltage across  $C_1$  **122** of the delay element **102** is zero. When the power amplifier **112** is powered on, the static reference current is turned on, in some examples to a value of 100  $\mu$ A. The control voltage **130** to the boost circuit **100** is also brought up to a desired value, in some examples to 3.3V. The transition of control voltage **130** may be coincident, slightly before, or slightly after the static reference current is turned on. The voltage across  $C_1$  **122** is still zero, which brings the gate voltage of the transistor **138** in the transconductance element **104** up to the control voltage **130**, which causes the transistor **138** to turn on. The source degeneration provided by  $R_2$  **140**, **142**, **144** limits the drain current,

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which allows for the current through transistor 138 to be approximately  $I_{BOOST, max} = (V_{CC} - V_{M1})/R_2$ , as discussed above.

With increasing time, the voltage across  $C_1$  122 increases with an inverse exponential characteristic. The rate at which the voltage across  $C_1$  122 increases is controlled by the value of  $R_1$  132, 134, 136. As  $C_1$  122 charges, the gate voltage of transistor 138 in the transconductance element 104 decreases exponentially, which causes the current that flows through transistor 138 to decrease exponentially as well. This decrease in the current that flows through transistor 138 generates an exponential decay of the output boost current. When the voltage across  $C_1$  122 becomes equal to  $V_{CC} - V_{Threshold\ voltage\ of\ M1}$ , which happens over time, transistor 138 turns off and the current through transistor 138 becomes zero. This change results in the output boost current decaying to zero and the bias current becomes equal to the static reference current, which is the desired steady state condition.

FIG. 3 is a graphical representation of the bias current over time 300 as it peaks to a value of the sum of the output boost current and the static reference current 302, then decays to a value of the static reference current 304. Referring again to the power gain of the power amplifier, the second amount of power gain provided by the power amplifier during a second time period after the power amplifier is powered on is determined by the exponential decay of the output bias current toward the value of the static reference current during the second time period. In some examples, the second time period begins when the second amount of power gain has reduced to a value acceptable close to the steady state amount of power gain. The first amount of power gain of the power amplifier is measured from the beginning of the first time period. The time constant can be defined as the amount of time between the initial powering on of the power amplifier (thus starting the first time period) and the time when the magnitude of the power gain of the power amplifier is close enough to its steady state value to induce an acceptable small error to the output signal. The power gain of the power amplifier is proportional to the exponential decay of the output bias current, as depicted in FIG. 3.

Referring now to FIG. 4, steps in a method 400 for correcting for a start-up transient in a power amplifier are shown. The steps include producing a boost current that has a decay characteristic 402, producing a static reference current 404, summing the boost current and the static reference current 406, and applying the summed boost current and the static reference current to bias a power amplifier 408. As discussed above, the power amplifier provides a first amount of power gain during a first time period after the power amplifier is powered on and a second amount of power gain during a second time period subsequent to the first time period after the power amplifier is powered on. The first amount of power gain is responsive to the sum of the boost current and the static reference current and the second amount of power gain is determined by the decay of the summed boost current to a value of the static reference current.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variations coming within the spirit and scope of the following claims.

The invention claimed is:

1. A circuit that corrects for start-up transients in power amplifiers, comprising:

a delay element arranged to produce a delay waveform signal responsive to an input voltage signal;

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a transconductance element having an input that receives the delay waveform signal from the delay element and is arranged to provide an output boost current based on the delay waveform signal and a gain of the transconductance element;

a reference element that provides an output bias current responsive to a static reference current and the boost current;

a bias element having an input that receives the bias current and is arranged to provide a bias control output; and

a power amplifier responsive to the bias control output and arranged to provide an amplified power output, wherein the power amplifier provides a first amount of power gain during a first time period after the power amplifier is powered on, the first amount of power gain responsive to the sum of the boost current and the static reference current and a second amount of power gain during a second time period after the power amplifier is powered on, the second time period following the first time period, the second amount of power gain determined by decay of the output bias current to a value of the static reference current.

2. The circuit of claim 1, further comprising a polarity inversion circuit having an input that receives the boost current and is arranged to provide an output that is a mirrored boost current, wherein the bias current is responsive to the mirrored boost current.

3. The circuit of claim 2, wherein the output bias current is the sum of the static reference current and the mirrored boost current.

4. The circuit of claim 1, wherein the second amount of power gain is determined by exponential decay of the output bias current toward the value of the static reference current during the second time period.

5. The circuit of claim 1, wherein the first time period begins when an enabling control signal is supplied to the power amplifier.

6. The circuit of claim 1, wherein the second time period begins when the second amount of power gain is 37% of the value of the first amount of power gain at a beginning of the first time period.

7. The circuit of claim 1, wherein the delay element includes a capacitor and at least one resistor that are electrically coupled in series.

8. The circuit of claim 7, wherein the delay element includes a first resistor, a second resistor, and a third resistor that are electrically coupled together in series and are digitally controllable.

9. The circuit of claim 1, wherein the transconductance element includes a switch and at least one resistor electrically coupled together in series.

10. The circuit of claim 9, wherein the transconductance element includes a first resistor, a second resistor, and a third resistor that are electrically coupled together in series and are digitally controllable.

11. The circuit of claim 1, wherein the output bias current is the sum of the static reference current and the boost current.

12. A method of correcting for a start-up transient in a power amplifier, comprising:

producing a boost current having a decay characteristic;

producing a static reference current;

summing the boost current and the static reference current; and

applying the summed boost current and the static reference current to bias a power amplifier, wherein the power amplifier provides a first amount of power gain during a first time period after the power amplifier is powered on,

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the first amount of power gain responsive to the sum of the boost current and the static reference current and a second amount of power gain during a second time period after the power amplifier is powered on, the second time period following the first time period, the second amount of power gain determined by decay of the summed boost current to a value of the static reference current.

**13.** A method of correcting for a start-up transient in a power amplifier, comprising:

producing a boost current having a decay characteristic, wherein the boost current is produced by a delay element having an input that receives an enabling control signal and is arranged to provide an output that includes a delay output signal and a transconductance element having an input that receives the delay output voltage from the delay element and is arranged to provide an output that includes the boost current that is based on the delay output voltage and a gain of the transconductance element;

producing a static reference current;

summing the boost current and the static reference current; and

applying the summed boost current and the static reference current to bias a power amplifier.

**14.** The method of claim **13**, wherein the delay element includes a switch and at least one resistor coupled together in series.

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**15.** The method of claim **13**, wherein the transconductance element includes a switch and at least one resistor coupled together in series.

**16.** A method of correcting for a start-up transient in a power amplifier, comprising:

producing a boost current having a decay characteristic, wherein the decay characteristic of the boost current causes the boost current to decay exponentially toward the value of the static reference current;

producing a static reference current;

summing the boost current and the static reference current; and

applying the summed boost current and the static reference current to bias a power amplifier.

**17.** A method of correcting for a start-up transient in a power amplifier, comprising:

producing a boost current having a decay characteristic, wherein the decay of the boost current begins when an enabling control signal is supplied to the power amplifier;

producing a static reference current;

summing the boost current and the static reference current; and

applying the summed boost current and the static reference current to bias a power amplifier.

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